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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/065,212	09/26/2002	Raj Kumar Jain	2000P19188US	8176

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HORIZON IP PTE LTD
8 KALLANG SECTOR, EAST WING
7TH FLOOR
SINGAPORE 349282, 349282
SINGAPORE

EXAMINER	
LE, THONG QUOC	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 11/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/065,212	JAIN, RAJ KUMAR	
	Examiner	Art Unit	
	Thong Q. Le	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 September 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20 and 22-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *2-10,13-20,22-25* is/are allowed.

6)☒ Claim(s) *1,11 and 12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Amendment filed on 09/11/2006 has been entered.

2. Claims 1-20,22-25 are presented for examination.

Response to Arguments

3. Applicant's arguments with respect to claims 1-20,22-25 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

5. Claims 1, 11-12 are rejected under 35 U.S.C. 102(e) as being anticipated by Hsu et al. (Pub. U.S. Patent No. 2002/0065997).

Regarding claim 1, Hsu et al. disclose an IC (Figure 3A) comprising:

a memory cell array (311-318) having a plurality of memory cells (Figure 1, 100), where each memory cells includes at least a first port and at least a second ports (Figure 1, [0054]), the first and second ports of the memory cells forming at least first and second access ports of the memory cell array for accessing the memory cells ([0039]);

a cache memory coupled to said first and second access ports ([0052]), wherein during a read operation to the memory cell array to obtain read data through one of said first and second access ports ([0052]), the cache memory provides file read data if the read data is contained therein or the memory cell array provides the read data if the read data is not contained in the cache memory ([0052]); and

a refresh control circuit for performing refresh operations for said memory cells ([0060]).

Regarding claims 11-12, Hsu et al. disclose wherein each memory cell (Figure 1, 100) of said memory cell array comprises a first selection transistor (Figure 1, 102) coupled to said first access port and a second selection transistor (Figure 1, 108) coupled to said second access port and a storage node (Figure 1, 110) connected to said first and second selection transistors, and wherein said storage node comprises a storage transistor (Figure 1, 104), a drain-source-path of said storage transistor being coupled between said first and second selection transistors, and a control terminal of said storage transistor being coupled to a reference potential (Figure 1).

Allowable Subject Matter

6. Claims 2-10, 13-16, 17-19, 20, 22-25 are allowed.

Claims 2-10, 17-19 include allowable subject matter since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Hsu et al. (Pub. U.S. Patent No. 2002/0065997), and others, does not teach the claimed invention having wherein said cache memory comprises a tag portion, an address portion, and a data portion corresponding to each other, wherein said tag portion indicates if said corresponding address and data portions contain valid address and data values as claims 2-10 disclosed, and a refresh control circuit to perform a refresh for the memory cells once within a retention time interval as claims 13-16 disclosed, and the second access port being controlled by a refresh control circuit to perform a refresh of the memory cells as claim 17-19 disclosed, and wherein the at least one of the first and second access ports used for memory access comprises an address path and a data read path, the address path connected to the address portion of the cache memory and the data read path of the at least one of the first and second access ports for memory access is connected to the data portion as claims 20, 22-25 disclosed.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thong Q. Le whose telephone number is 571-272-1783. The examiner can normally be reached on 8:00am-5:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zarabian Amir can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Thong Q. Le
Primary Examiner
Art Unit 2827

10/31/2006